# Lab Manual 14

# Counters

## Objectives:

Students should be able to design counters using Flip-Flops

## Counters

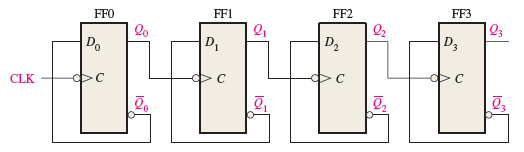
A counter is a register that goes through a predetermined sequence of states upon the application of clock pulses. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip flops. In a synchronous counter, the clock inputs of all of the flip flops receive the common clock pulse, and the change of state is determined from the present state of the counter.

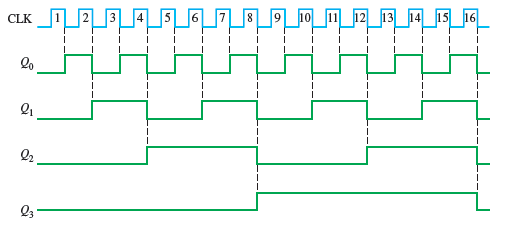
## Problems / Assignments

**Note: You don’t need to submit written work. Don’t use clock generator instead use binary switch for clock for both the questions.**

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| **Problem 1** |  |

Implement a 4-bit an asynchronous binary counter with D flip flops **(negative edge-triggered**).

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| **Problem 2** |  |

Design and implement 3-bit synchronous up/down counter using JK flip flops. If selection ‘Sel’ is 0, it counts from 0 to 7 and repeats. If selection is 1 it counts downwards from 7 to 0 and repeats.

**Hint: Employ design method for sequential circuit taught in theory class.**